THE KENYA POLYTECHNIC

ELECTRICAL/ELECTRONICS ENGINEERING

DEPARTMENT

HIGHER DIPLOMA IN ELECTRICAL ENGINEERING

END OF YEAR II EXAMINATIONS

NOVEMBER 2006

DIGITAL ELECTRONICS

3 HOURS

INSTRUCTIONS TO CANDIDATES:

You should have the following for this examination:

Answer booklet

Calculator/Mathematical tables

Answer any FIVE of the following EIGHT questions.

All questions carry equal marks and the maximum marks for each part of a question are as shown.

This paper consists of 5 printed pages.

1. (a) Define the following terms with reference to Karnaugh maps:

   (i) Prime implicant (ii) Essential prime implicant

   (iii) Non-essential prime implicant (3 marks)

   (b) Determine the minimum sum of products solution for the function:

   $F(A,B,C,D) = \Sigma m(0,1,3,5,6,7,8,10,14,15)$ (8 marks)

   (c) Using a five-variable K-map, simplify the function:

   $F(A,B,C,D,E) = \pi(1,3,5,7,8,10,12,14,16,18,19,20,22,23,24,26,28,30)$ in:

   (i) Sum of products (ii) Product of sums (9 marks)

2. (a) (i) Express the Boolean function $F = AB + \overline{A}C$ in a product of maxterm form.

   (ii) Using the result in (a)(i) or otherwise, obtain the expression for the sum of minterms for the function. (7 marks)

   (b) Use Boolean algebra to show that an X-OR function, F, with four variables is made up of the indicated minterms.

   $F(A,B,C,D) = \Sigma M(1,2,4,7,8,11,13,14)$ (5 marks)

   (c) Using double complement method, use NOR gates only to realize the function $F = A(B + CD) + B\overline{C}$ (8 marks)

3. (a) Using AND and OR gates, find a minimum network to realize:

   $F(A,B,C,D) = M_0 M_1 M_3 M_{13} M_{14} M_{15}$

   (i) Using two logic level (ii) Using three logic level

   [Number of gates and gate inputs are the design parameters] (10 marks)

   (b) (i) Find the minimum network of two-input AND and two-input OR gates to realize: $F(A,B,C,D) = \Sigma m(0,1,2,3,4,5,,7,9,11,13,14,15)$

   (ii) Convert the network in (b)(i) to two-input NAND gate using direct polarity notation. Add inverters where necessary. Assume that only A(L), B(H), C(L) and D(H) are available as inputs and that the output should be F(H). (10 marks)

4. (a) (i) Explain how a decoder can be used for memory address decoding.

(ii) A ROM has n input lines and m output lines. Write down the expression for the capacity of the ROM. (6 marks)

(b) (i) Draw the logic diagram of a 4-to-1 multiplexer.

(ii) Explain the operation of the multiplexer in (b)(i). (8 marks)

(c) Implement the function $F(A,B,C) = \Sigma(1,3,5,6)$ with a 4x1 MUX with:

(i) B and C connected to the selection lines S_1 and S_0 respectively.

(ii) A and B connected to the selection lines S_1 and S_0 respectively.

(6 marks)

5. (a) Distinguish between synchronous and asynchronous logic. (2 marks)

(b) (i) Design a counter that has a repeated sequence of six states as listed in table 1. [Use J-K flip-flops]

Count Sequence

A	B	C
0	0	0
0	0	1
0	1	0
1	0	0
1	0	1
1	1	0

Table 1

(ii) By use of a state diagram, show that the counter in (b)(i) is self-starting. (10 marks)

(c) A combinational circuit is defined by the functions:

$F_1(A,B,C) = \Sigma(3,5,6,7)$

$F_2(A,B,C) = \Sigma(0,2,4,7)$

Implement the circuit with a PLA having three inputs, four product terms and two inputs. (8 marks)

6. (a) Compare any TWO characteristics of a practical operational amplifier to that of ideal one. (2 marks)

(b) (i) Figure 1 shows a binary weighted resistor D/A converter. Show that the:

I. Output resistance is independent of the digital word and that $R_0 = \frac{2^{N-1}}{2^N - 1} R$

II. Analog output voltage for the MSB is $V_0 = \frac{2^{N-1}}{2^N - 1} U_R$

III. Analog output voltage for the least significant bit is

$$V_0 = \frac{1}{2^N - 1} V_R$$

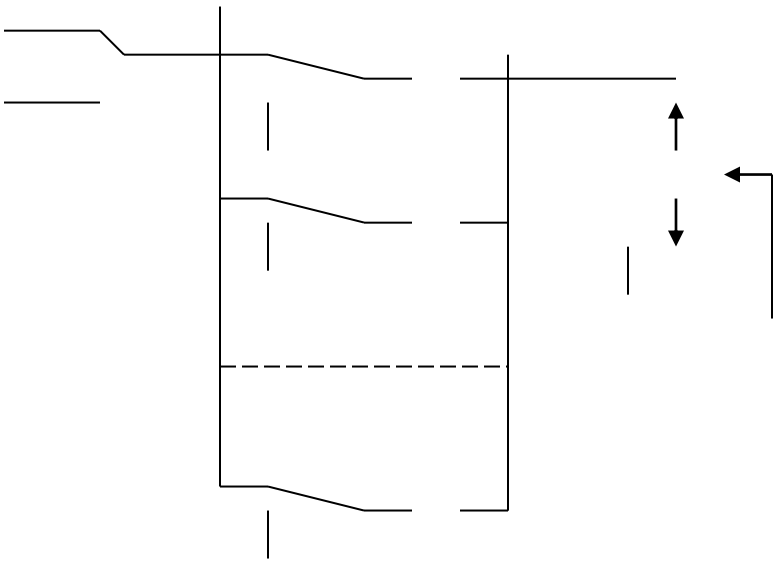
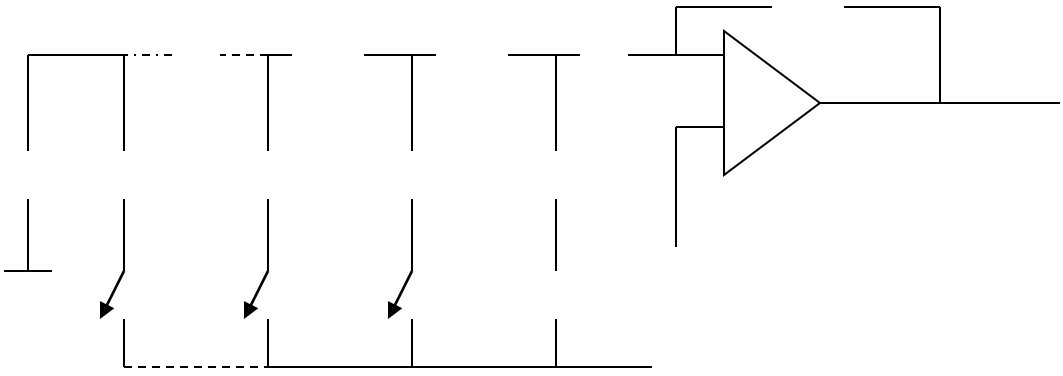


Figure 1

(ii) Explain the main disadvantage of the binary weighted ladder.

(12 marks)

(c) Figure 2 shows a R-2R D/A converter network.



Find the expression for V_0 if only the:

(i) The MSB is ⊥ (ii) The third MSB is ⊥

(iii) The LSB is ⊥ (6 marks)

7. (a) distinguish between the following modes of data transfer:

(i) Serial and parallel

(ii) Asynchronous and synchronous (8 marks)

(b) Describe the function of the VART in peripheral communication. (4 marks)

(c) Describe the basic operation, recording format, data density and capacity of:

(i) Hard disk (ii) Floppy disk (8 marks)

8. (a) Assume that only a J-K flip-flop is available. Draw a diagram that includes a J-K flip-flop and one or more logic gates to construct:

(i) A D-flip-flop (ii) A T-flip-flop (4 marks)

(b) A microprocessor (mp) outputs three control signals that have the meaning given in the following table. [No knowledge of mp is necessary to solve this problem]

R′	W′	M/I′O′	
0	1	1	mp wants to read memory
1	0	1	mp wants to write memory
0	1	0	mp wants to read an input/output device
1	0	0	mp wants to write to an input/output device
1	1	X	mp wants non of the preceding operations

(i) Design a logic circuit using a suitable multiplexer and minimal additional logic to transform these three signals into the following four signals, each representing an operation:
(MR)′, (MW)′, (IOR)′, (IOW)′
When any of the operations is desired (not desired) the values of the corresponding signal is to be 0(1). (8 marks)

(ii) Design a multiplexer implementation to perform the inverse transformation. (8 marks)